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FAST EDGES
SIGNAL INTEGRITY SPECIALISTS

Signal / Power Integrity and High Speed Design
Class Agenda

What is a transmission line
- What causes transmission lines
- What do they do to digital circuitry
- Avoiding transmission line problems

Transmission line effects
- Undershoot & Overshoot – can destroy boards
- Ringback, monotonicity, crosstalk, timing

Printed circuit boards
- Stackup
- Making controlled Zo, not controlled spacing
- What you get is not what you think
- Crosstalk problems with multiple vendors

Drivers, receivers, Zo
- Strength & speed
- Zo & drivers
- Incident vs reflected wave switching

PCB interconnect delay
- Different than system delay but important
- Receiver input C, driver output Rs, PCB Zo, etc
- Reflected vs incident wave switching

Termination
- Placement and stub length
- Parallel, series, Zo matching, driver Rs matching
- Diodes - dangerous

Topologies
- When are topologies important
- How do topologies affect signal integrity & timing
- Short & long Tee, star, daisy chain
- Stub length

Package parasitics

- L's, C's, and R's
- Transmission lines in packages
- How do they affect signal integrity & timing
- Capacitive loading on transmission lines

S Parameters

- Frequency dependent descriptors
- Good for gigahertz designs
- S_{21} - Insertion loss or interconnect loss for SI
- Includes discontinuities, connectors, packages
- VNA - 2 & 4 port networks
- S_{21}, S_{41} & S_{31}
- S_{dd21}, S_{dd41} & S_{dd31}

Differential pair – multi Gb/s

- Noise and EMI
- Layout issues
- Zdiff, Zcomm, Zeven, & Zodd
- Controlling Zdiff
- Side to side vs broadside (over/under)
- Weak vs strong coupling
- Zdiff problems
- Skew affects on signal integrity & timing
- Better terminations
- Pad & antipad issues
- Routing rules
- Controlling mounting & gold finger capacitance
- How to make high speed differential pair vias

Crosstalk

- What causes crosstalk
- Safe routing densities
- Effects on timing & signal integrity
- Microstrip vs stripline - different
- Side to side vs broadside (over/under)
- FEXT vs NEXT
- Effects of Zo, trace width, spacing, length, guard tracks & more
- Differential pair crosstalk
  - Diff pair to diff pair
  - Diff pair to single ended signals
- Fixing crosstalk
- What needs to be done by layout designers

PCB power integrity

Planes

- Power & ground
- Spacing & location - loop inductance

Bypass capacitors

- ESL
- Package & size µF
- Spacing to load
- Location on PCB & empty spaces
- Mounting inductance, via placement, spacing, pads

Reference planes

- Perforation
- Crossing splits
- Reference consistency in designs
- Vias, layer changes & references
- Controls routing & stackup
- Need to inform layout designers

Connectors

- Controlled Zo, geometry, pinouts
- Reference consistency
- How many grounds & Vccs - return currents

Vias

- Zo changes
- Reference changes
- Diff pair stub lengths
- Blind & buried vias
- Pads, antipads, hole diameter
- Loading
- How to make a multi-GHz via

AC losses

- Skin effect
- Dielectric loss - D_F or tan(δ)
- Microstrip vs stripline
- Noise margins with differential pair
- Pre-emphasis & equalization
- Surface coatings / treatment

Fiber Weave Effect – FWE

- Multi Gb/s problems
- Different weaves, different spacing

- Routing for skew – angles & spacing
- Materials available

Trace surface roughness

- Causes
- Additional losses
- Options from PCB manufacturers

Testing issues

- Faster boards are harder to test
- How do you test high speed boards
- What equipment & how fast

IBIS models

- Drivers & receivers
- Simulators & accuracy
- Repairing & modifying
- Rs, t_{rise} / t_{fall}, input C, parasitics

Layout issues

- How to make quality high speed boards
- What tools are needed
- Signal integrity issues must be included
- PCBs are now part of the design
- Engineer / layout cooperation